Thermal Fatigue Results for Surface Mount Devices Using Resistance 'I'racking and Intermittent Current Detection Electrical lest Methods

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Abstract:
Thermal fatigue life testing of various electronic packaging technologies is being performed by the Reliability Technology Group at the Jet Propulsion Laboratory. These testing efforts are in progress to improve understanding of the reliability issues associated with low volume packaging technologies for space applications and to develop qualification and acceptance approaches for these technologies. This work discusses the electrical failure detection techniques used during long term thermal cycle testing, and it provides a summary of current test results for thermal cycle induced fatigue failures. Failure data will be presented for thermal cycles of different temperature ranges and means. Only 68-pin and 28-pin leadless packages have shown failures to date. The 68-pin leadless have all failed, the 28-pin leadless have not yet all failed and the J-lead and gull-wing package types have shown no failures to date (up to a maximum of 1700 cycles). For the leadless packages, failure data obtained for different thermal cycle environments will be presented. A currently unexplained phenomenon related to test vehicles tested one year apart over the same temperature range is also discussed. In addition, results of electrical probing to localize failure location and a comparison of both intermittent and resistance measurements is given.

Keywords: fatigue, surface mount, measurement, testing, thermal cycling, intermittent detection, acceleration factors, cold-biased cycling

Introduction / Background:
The Reliability Assessment Technology Testing Laboratory at the Jet Propulsion Laboratory is dedicated to the qualification and reliability assessment of advanced technologies and designs for space-flight applications. In addition to other ongoing work, life testing of surface mount technology (SMT) components is currently in progress. The principle failure mode being addressed is that of thermal fatigue of solder joints due to stress induced by coefficient of thermal expansion (CTE) mismatches between component and board during thermal cycling. Life testing of surface mount devices is not new, but the current effort explores the relationship between reliability and various parameters for ultra low volume applications. The goal of the work presented here is to address the following issues: electrical test methods, failure location, cold biasing of temperature cycle, and power laws for 68 pin and 28 pin leadless surface mount devices. The life test i ng was performed for two room temperature centered temperature ranges (-25 to 95 °C and O to 80 'C) and a cold-biased cycle (-55 to 2S 'C).

Test Articles:
The SMT RTOP board as shown in Figure l was designed specifically for SMT life testing. Efforts were made to perform testing on a "real-life" board while taking steps to isolate the solder joints as the driving life parameter. The steps taken to achieve this were: all connector pins are redundant, all signal traces are on the top or bottom layers, wire-bonds are all double-stitched, and all vias used to go from the top to bottom layer are triply redundant. The board is seven-layers to ensure copper balancing and provide a realistic composite CTE. The board material is polyimide. Furthermore, the board backside allows electrical probing to each lead to determine exactly where the solder joint failure occurred (to one of two solder joints). The top layer of the board is shown in Figure 1. Thirty-five test boards are being subjected to various test environments as part of a complete design of experiments.

Experimental Setup and Failure Detection:
The test articles and measurement techniques have been described previously' but include both intermittent and DC resistance measurements for a variety of daisy-chained package types. The resistance tracking circuit is essentially a 4-point resistance measurement across a daisy chained component, and the intermittent measurement detects a voltage change across an in-series resistor which latches a digital logic circuit; this is triggered at resistance spikes of approximately 150 ohms. These measurements

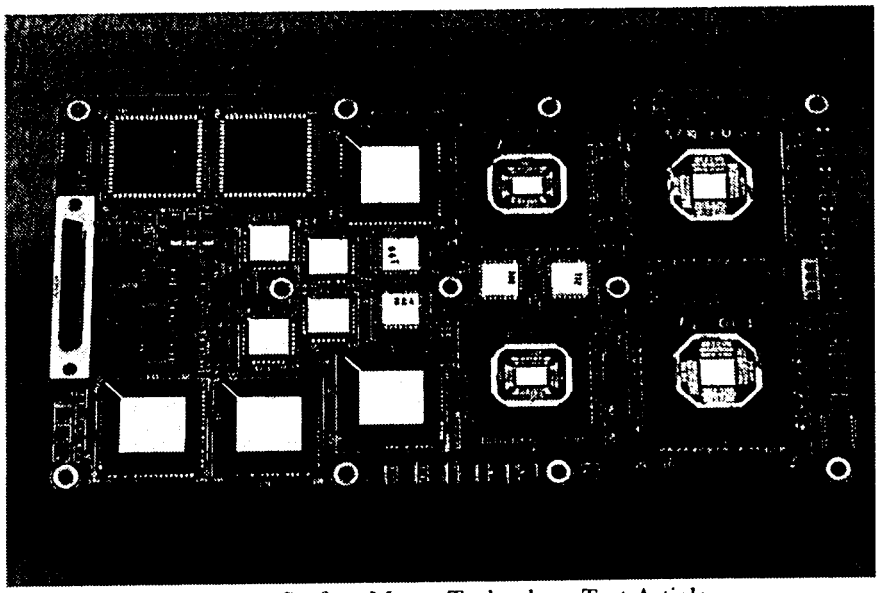


Figure 1: Surface Mount Technology Test Article

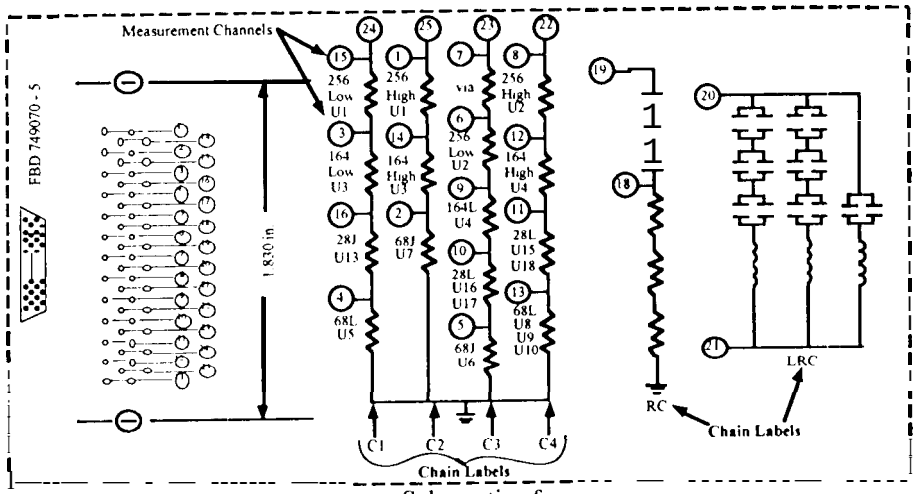


Figure 2: Electrical Schematic of SMT Test Article

were part of' an automated data acquisition and control system with human intervention only after 1) prc-planned inspection points 2) detected failures or 3) equipment problems. Figure 2 is a schematic representation of the SMT RTOP board shown in Figure 1. Each resistor represents the daisy chained component(s) to be measured. Due to the large number of components and the relatively small number of available pin connections some sacrifices in resolution were made. For instance, some of the automate resistance tracking measurements were made on multiple parts, although isolation to individual leads can be achieved manually. Four intermittent open measurements arc mad con the board, one per each chain.

Failure Location Documentation

Electrical resistance and intermittent measurements were done on daisy chained components as discussed above. In addition, failure site determination was performed by electrical probing on backside pads to minimize intrusive effects; probing gives resolution into failure of one of two joints. In some cases, the failure site was not uniquely identified due to failures at multiple sites. Multiple failure sites occur since cylic tests arc started for a fixed number of cycles; probing does not take place until the end of the cyclic test while electrical measurements are continuous. Because solder joint fatigue life for leadless devices is driven by (among other factors) the CTE mismatch between the package and the substrate, the first failures

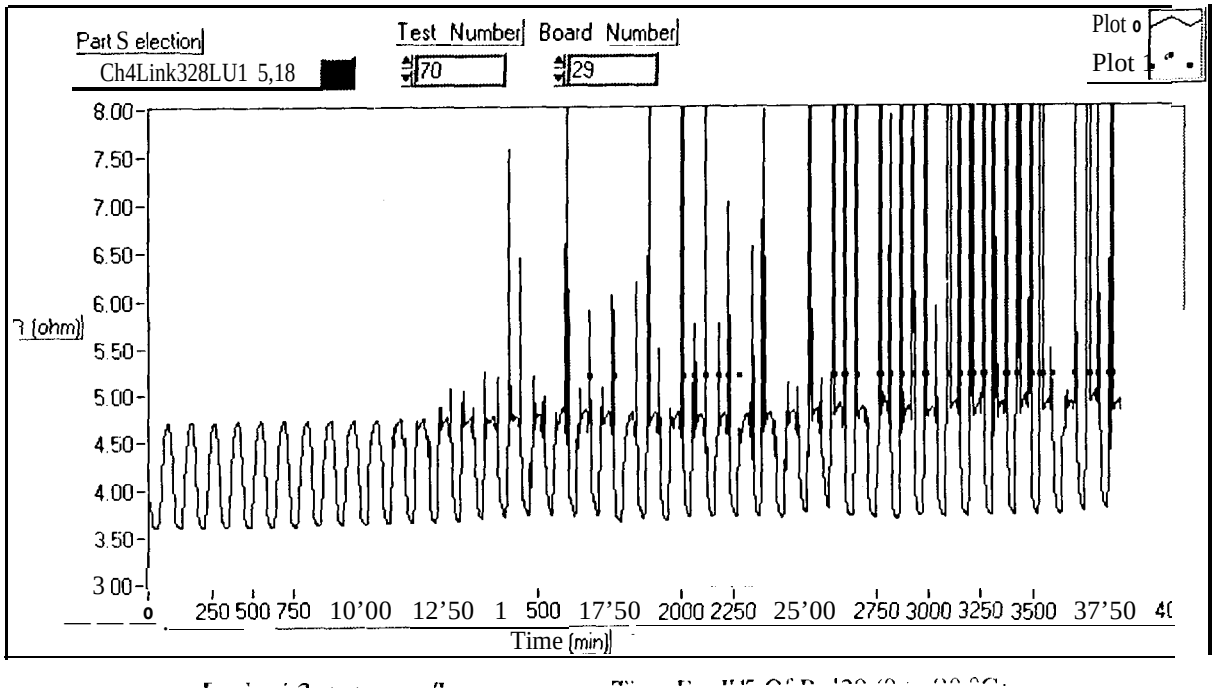
were expected to occur at the corners of the packages where the CTE-induced relative displacement between substrate and package is greatest. Because of variations in the solder joints themselves some failures could be expected to (and did) occur at non-corner locations. For the 68-pin leadless devices in second phase of testing and the -55 to 25 'C environment, 9 out of 9 components had failure sites that were isolated to onc probe location and in all 9 cases the joint was at a corner pin; an additional 3 components had multiple failure sites (which included corners). In contrast to this, 8 components for the second phase of O to 80 "C testing, 2 were isolated to corners, 1 was isolated to a middle joint, and 5 had multiple failure sites on corner and middle leads. Similar results were seen in the first phase of testing. 28 leadless failure location probing was inconclusive as there arc so fcw leads on a package side. Work is continuing to correlate these measurements to initial solder joint assessments of quality.

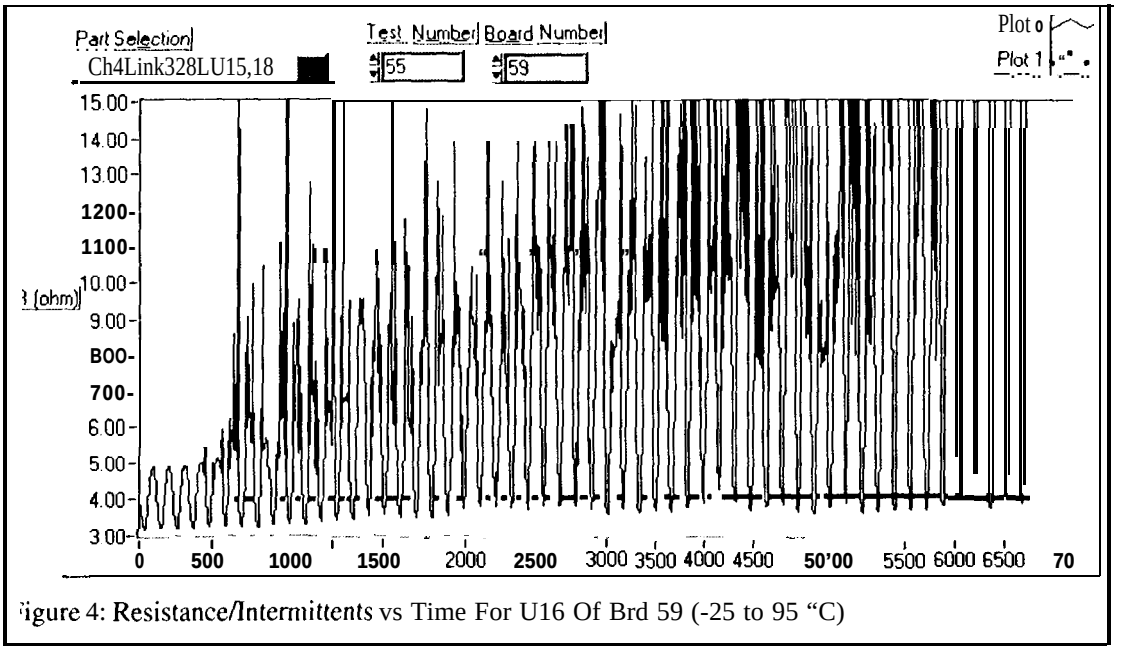
Resistance vs. Intermittent

Sources in literature have often reported the importance of intermittent open detection as essential in assessing the electrical performance of solder joints under thermal cyclic loading[2,3,4,5,6]. Therefore, this testing combines intermittent open detection with resistance tracking measurements in hopes of providing greater resolution into the onset of failure of surface mount devices. Electrical resistance measurements of daisy chained components and intermittent current detection circuitry provided similar results for leadless component failures. For 68 leadless components, the resistance tracking measurements used provided little warning for upcoming solder joint opens. Intermittent measurements flipped logic state at resistance threshold ranging from 130 to 250 ohms (dependent on specific circuit and bow-d), while electrical resistance measurements could measure resistance to less than 10 mini-ohm. In some cases, small resistance fluctuations were seen 5 cycles before intermittent; however, in the majority of cases, resistance fluctuations were not seen before 1 cycle of the first intermittent. However, this was not true for the 28 leadless where resistance fluctuations were seen before intermittent. Examples of such are shown in Figure 4, Figure 3, and Figure 5. The dots marked "Plot 1" in the legend represent where intermittent occurred. The x-axis is time in seconds. The time is not the total time in test, but rather the time for a particular

Table 1: Resistance vs Intermittents For 28 leadless

Cyclic Temperature Range	Average Number Of Cycles Resistance Fluctuations Were Seen Before Intermittents	Percentage of Total Number of Cycles In Which Resistance Fluctuations Were Seen Before Intermittents
-25 to 95 "C	4.4	.7
0 to 80 "C	8.4	.8
-55 to 25 "C	28.25	2.8





'igure 4: Resistance/Intermittents vs Time For U16 Of Brd 59 (-25 to 95 "C)

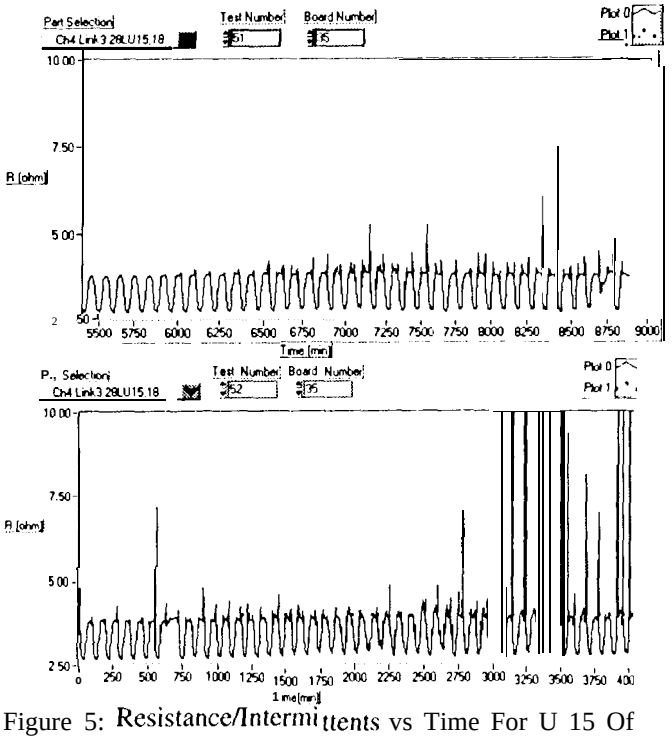


Figure 5: Resistance/Intermittents vs Time For U 15 Of Brd35 (-55 to 25 "C)

test number which is used as a test conductor reference only. While some advanced warning is given by the resistance tracking measurement, the intermittens detection measurements are closely correlated to DC detected "failures." While the resistance tracking measurements do not appear useful for reducing life testing by a significant amount as initially hoped, in-situ resistance measurements may provide some small early warning for critical spacecraft functions.

Background On Cumulative Distributions/Power Laws:

Much of the data presented in this paper will be in the form of cumulative plots, where the abscissa is the fraction of the total population failed and the ordinate is the cycle at which the failure occurred. These plots are useful for fitting to distribution functions which yield a variety of information including the number of cycles to mean failure and the spread between the first and the last failure. Comparisons can then be made between different part types, geometry, test environments, etc., using time (or number of cycles) to first failure or to mean failure, etc. For the purposes of spaceflight operation, it is the time to first failure that counts: the spacecraft function has failed long before 50% of the components have failed! The shapes of the distributions can be used to establish design margins to reduce the probability of the first failure occurring during the mission. The usual distribution to fit the data to is the two-parameter Weibull distribution:

$$P(N) = 1 - e^{-(N/c)^m}$$

where c is the number of cycles to 63% failure and m is the shape parameter, or exponent, which characterizes the slope of the cumulative plot. It is usual for leadless packages m have values of m up to 8.0 which reflects the ability to uniformly control the production of these types of solder joints, while values for m remain below 4 for most leaded devices.

Comparisons can also be made between populations which were cycled over different temperature ranges to obtain acceleration factors. This is important for life testing to simulate usage environments where one does not have schedule or resources to test for 5 to10 years. Thus, one would like m simulate solder joint fatigue failure over a great number of small amplitude temperature cycles by doing a fewer number of cycles over a greater amplitude temperature cycle. Acceleration factor, or power law exponents, are widely found in literature[7,8,9,10,11] and arc a subject of some controversy since reported values range from 1.4 to 2.6 and higher. Some of the disagreements can be explained by different test conditions, model types, definitions of failure, etc. but disagreement still remains[9]. In the simplest models, one starts with the Coffin-Manson[7] fatigue equation and derives the equation:

$$\frac{N_2}{N,} = \left(\frac{T_1}{T_2}\right)^{\alpha}$$

Where N, and T_1 are the number of cycles to failure and the temperature cycle amplitude, respectively for a particular cycle test and N_2 and T_2 are similarly defined for another cycle test. α the fatigue exponent and is approximately 2.0 for single-phase materials in the Iow-cycle fatigue regime'.

Effect of Cold-Biased Cycling:

In an effort to understand the effects of mean temperature on cyclic fatigue, "identical" test articles were exposed to both O to 80 °C and -55 to 25 "C thermal cycles. Literature has predicted opposite effects[9]; some say a lower mean will decrease creep and therefore increase life, while others claim that at lower temperatures the solder ductility will decrease which is essential duc [o the constrained nature of leadless packages which will therefore decrease life. Figure 6 shows life distributions for each of these test environments obtained from recent experimental data; with this limited data set it appears that the life of leadless components for the temperature ranges under consideration is not dependent on temperature biasing. Figure 7 shows failure distributions of 28 leadless components with the same environments. The life for the 28 leadless does increase slighty for the lower temperature bias cycle, but the shift is relatively small. In addition, resistance tracking measurements as discussed earlier detected fluctuations before intermittents on a more significant scale for the cold biased cycles. Furthermore, electrical probing was more conclusive to individual leads for the cold-biased cycle data as well. The combination of the three different measurements suggest there is definitely a difference between the actual failure mechanism between the different cyclic temperature ranges, despite the fact that the distributions arc relatively close for the cycles considered. With this in mind, care should be taken in extrapolating this data to lower or higher temperature means or other part configurations (i.e. gullwing, leadless, BGA), as the difference in failure mechanisms is currently not understood, and more drastic effects may occur with other configurations. It is important to note that these boards were subjected to thermal cycling only; combined vibration as the real operating condition may yield somewhat di fferent results, due to solder stiffness changes with temperature.

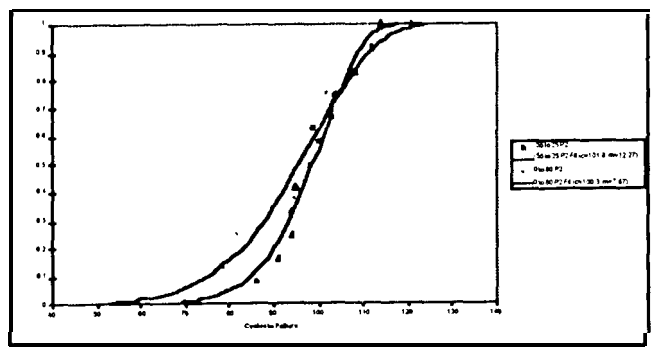


Figure 6: 68 Leadless Failure Distributions For O to 80 "C and -55 to 25 "C

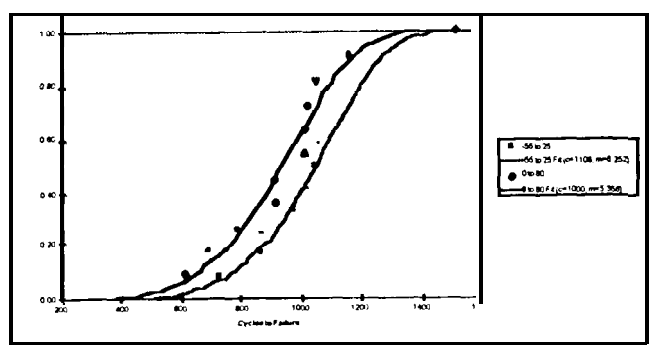


Figure 7: 28 Leadless Failure Distribution O to 80 "C and -55 to 25 'C

Power Law:

Figure 8 plots the cumulative failure data for the 68-pin leadless device failures for two cycles: -25 to 95 "C and O to 80 'C. Note that the fatigue exponent derived from this data is 1.7 (using the 50% failure point), which is consistent with other reported values.

Figure 9 plots the same data for the 28-pin leadless devices and now something unusual is observed -- the power exponent is approximately 1.0, which was unexpected. Careful examination of the data revealed that this testing was all done in the first phase of testing. On the other hand, the 68-pin data was obtained by combining the results from both a first and second phase of testing (which

began one year after the first phase). The test articles were all "identical" in that [hey were fabricated from the same parts, with the same processes, by the same vendor and at the same time. The only differences between the two test phases were the onc year lag and the lack of inspection steps in the second phase, which was done completely automated[1]. To explore the hypotheses that the second phase results were somehow different than the first phase, the 68-pin failure data was replotted as two separate populations as shown in Figure 10. Now it is clear that the first phase data again had a fatigue exponent of 1.0 (like the 28-pin data) and the second phase data had a fatigue exponent of 2.0 which is more consistent with literature values.

The second phase of testing also included -5S to 25°C Cycles. Figure 11 shows that the distribution shift discussed above occurred for both the O to 80 "C and -55 to 25 °C cycles, but it was more significant for the O to 80 °C cycle. Note that the cold-biased cycle failed later than the room-temperature-centered cycle (O to 80 °C) in the first phase of testing than it did in the second phase.

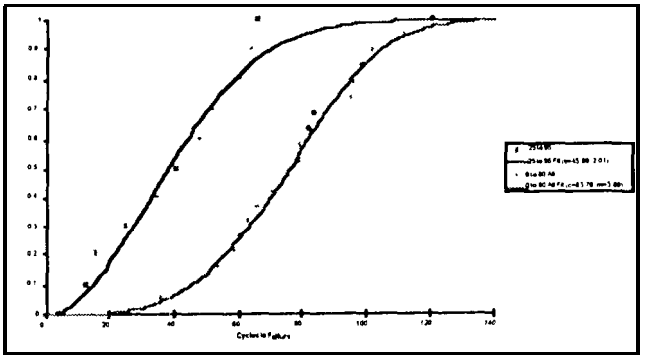


Figure 8: 68 Leadless Failure Distributions For -25 to 95 "C-and O to 80 "C

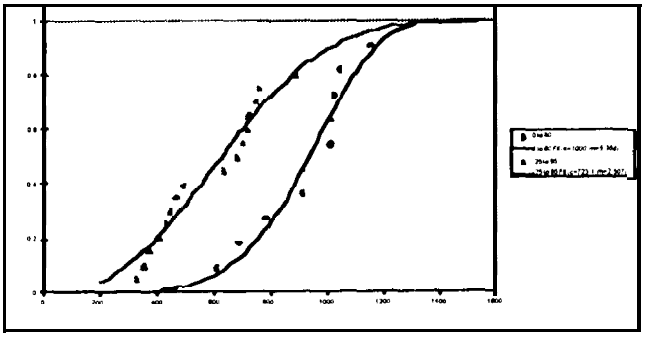


Figure 9: 28 Leadless Failure Distributions For -25 to 95 "C and 0 to 80 "C

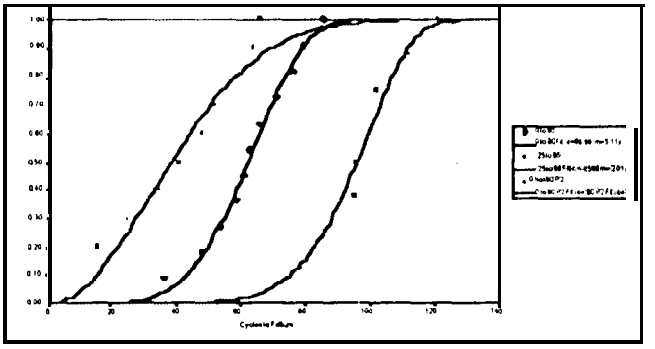
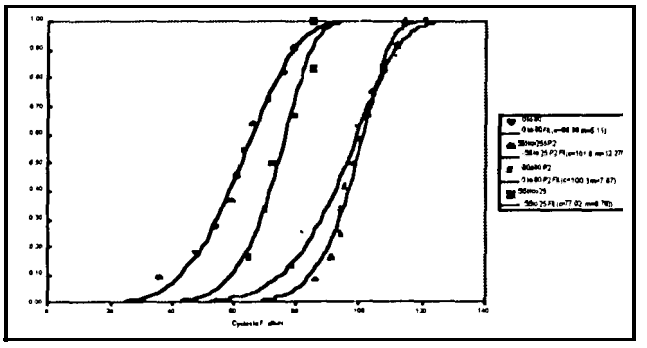


Figure 10: 68 Leadless Failure Distributions -25 to 95 °C and Split Phases of the O to 80 'C Cycle Tests



Fi.cure 11: Failure Distributions For Both Sets of O to 80°C and -55 to 25°C Distributions

Conclusions:

In the presented results, the failure distribution for O to 80 'C thermal cycles compared rather closely to the distribution for -55 to 25 'C thermal cycles for both 68-pin and 28-pin leadless devices. However, there was a slight increase in life with the low temperature biased cycle for the taken taken in the first phase of testing. In addition, electrical resistance measurements detected fluctuations before intermittent much earlier in the -55 to 25°C than in the room temperature biased cycles, and electrical probing for solder joint failure isolation was more conclusive for the low temperature biased cycle. These results yield that there is a difference in the failure mechanism due to temperature biasing of thermal cycles. The significance of these results may be much greater for other package configurations. A disturbing fact in the testing was the shift in life distributions for the 68 leadless components which underwent an additional year of aging. Comparing -25 to 95 "C cycle data to O to 80°C data taken at approximately the same time to additional O to 80 °C data taken a year later yields two distinct power laws of 1.0 and 2.0. This phenonmena is not yet understood, but it may provide insight into the spread of literature data. Furthermore, resistance and intermittent measurements for

both 68 and 28 leadless data yielded similar results: the resistance tracking measurements only provided limited warning of failure, but [his may prove to be sufficient for critical applications.

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